REMARKS

Claims 1-3, 18-21, 37-53, and 58-64 are pending in the subject application. Claims 37-53 and 58-64 were withdrawn from consideration as being directed to non-elected subject matter. Claims 1-3 and 18-21 have been amended by the present amendment. The amendments are fully supported by the application as originally filed.

In the Office Action of 08/31/2005, the drawings were objected to because the term "the pulse signal" was used to designate both a first input and an output in claim 1. A similar objection was made with reference to claim 18. In the Office Action, it was stated that these signals "are two different pulse signals" which should be referenced using different reference characters (see page 2 of Office Action dated 8/31/2005). The Examiner also objected to the specification and rejected the claims under 35 USC 112, second paragraph, as being indefinite.

As amended, claim 1 recites a first input terminal into which the pulse signal is inputted; a second input terminal into which the clock signal is inputted; and an output terminal from which a synchronized pulse signal is outputted. Claim 1, as amended, refers to two different "pulse" signals: a pulse signal, which is inputted to the first input terminal, and a synchronized pulse signal, which is outputted from the output terminal.

The specification and drawings clearly describe a latch circuit and a shift register circuit having a plurality of latch circuits, as recited in claims 1 and 18, with reference to the embodiment shown in FIGS. 1-4 of the application.

For example, as shown in FIG. 2 of the application, a latch circuit includes a first input terminal IN into which a pulse signal is inputted and a second input terminal CK into which a clock signal is inputted (see specification at page 86, lines 7-10). FIG. 2 also shows an output node OUT from which a synchronized pulse signal is outputted, i.e., the latch circuit "transmits the pulse signal in synchronization with the clock signal" as the output (page 11, lines 21-24). Therefore, the first input terminal, second input terminal, and output terminal, as well as the

inputted pulse signal and the outputted synchronized pulse signal are clearly described in the specification and shown in the drawings.

Regarding the rejections under 35 USC 112, second paragraph, claim 1, line 3 refers to "the pulse signal" which has proper antecedence to "a pulse signal" in the preamble of claim 1. Similarly, in claim 1, line 4, "the clock signal" has proper antecedence to "a clock signal" in the preamble of claim 1.

Claims 1-3 and 18-20 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 15, and 23 of U.S. Patent 6,580,411 to Kubota et al.

It is believed that the claim amendments as provided herein obviate the double patenting rejection. Therefore, a Terminal Disclaimer has not been filed at this time.

Claims 1-3 and 18-20 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,894,296 to Maekawa (hereinafter "Maekawa '296") in view of U.S. Patent 5,646,642 to Mackawa et al. (hereinafter "Maekawa '642"). This rejection is respectfully traversed.

The Maekawa '296 reference is directed to a bidirectional signal transfer shift register with a multi-stage structure including a plurality of flipflops FF, each having an input terminal IN and an output terminal OT, where the input and output terminals of the flipflops are connected successively (see column 5, lines 33-39).

On page 7 of the Office Action of 08/31/2005, it was admitted that Maekawa '296 does not teach or suggest the use of a clock signal having an amplitude smaller than an amplitude of the pulse signal, or a clock signal input control section which inputs and stops the supplied clock signal.

The Maekawa '642 reference was cited allegedly for teaching the use of (i) clock signals CK1 and CK2 which have amplitudes smaller than amplitudes of pulse signals VA and VB; and (ii) clock signal input control sections 1A and 1B to input and stop the supplied clock signal (see Office Action of 08/31/2005 at page 7, last full paragraph).

However, in Mackawa '642, the signals VA and VB are mere potentials which vary depending on the clock signals CK1 and CK2 at points A and B in the circuit shown in FIG. 1 (see also FIG. 2 of Maekawa '642; and column 5, lines 62-66). However, the signals VA and VB do not correspond to the "pulse signal" recited in claim 1, which is inputted independently of the claimed "clock signal."

In other words, the circuit disclosed in FIG. 1 of Maekawa '642 has only input terminals for the clock signals CK1, CK2, and does not teach or suggest a "second input terminal" for receiving a pulse signal, as recited in claim 1.

Consequently, the output signal Vout shown in FIGS. 1 and 2 of Maekawa '642 is merely the clock signal CK1 in the same phase amplified nearly to the level of supply voltage VDD (see column 5, lines 64-66), which does not correspond to the Applicants' claimed "synchronized output pulse" outputted from an output terminal, as recited in claim 1. Although the output signal Vout has a larger amplitude than the clock signal CK1, it is not derived from a pulse signal, as recited in claim 1.

For at least the reasons discussed above, the Maekawa '642 reference could not be combined with Mackawa '296 to somehow produce the Applicants' claimed invention, as recited in claim 1.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Applicants believe that additional fees are not required for consideration of the within Amendment. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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